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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Applicant Initiated Interview Request Form

Application No.: 10/587,608 First Named Applicant: Pessolano

Examiner: Pathak, Sudhanshu Art Unit: 2611 Status of Application: pending

Tentative Participants:

(1) Sudhanshu Pathak (2) Mark Wilson, 43,994

(3) _____ (4) _____

Proposed Date of Interview: 2/23/2010 **Proposed Time:** 11am **AM/PM**

Type of Interview Requested:

(1) ☑ **Telephonic** (2) ☐ **Personal** (3) ☐ **Video Conference**

Exhibit To Be Shown or Demonstrated: ☐ **YES** ☑ **NO**

If yes, provide brief description: _____

Issues To Be Discussed

Issues (Rej., Obj., etc)	Claims/ Fig. #s	Prior Art	Discussed	Agreed	Not Agreed
(1) amendment	1	Liu et al.	☐	☐	☐
(2)			☐	☐	☐
(3)			☐	☐	☐
(4)			☐	☐	☐

☐ Continuation Sheet Attached

Brief Description of Argument to be Presented:

Discuss proposed amendment of claim 1 as provided on attached page.

An interview was conducted on the above-identified application on _____ .

NOTE: This form should be completed by applicant and submitted to the examiner in advance of the interview (see MPEP § 713.01).

This application will not be delayed from issue because of applicant's failure to submit a written record of this interview. Therefore, applicant is advised to file a statement of the substance of this interview (37 CFR 1.133(b)) as soon as possible.

/mark a. wilson/
Applicant/Applicant's Representative Signature

Mark A. Wilson
Typed/Printed Name of Applicant or Representative

43994
Registration Number, if applicable

Examiner/SPE Signature

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) An electronic device for generating a clock signal for an integrated circuit, the device comprising:

at least two clock generation elements configured to generate a single clock signal at a clock output in response to an input signal and to operate in a mutually exclusive manner, the outputs of said clock generation elements being selectively connectable to said clock output;

means for receiving a data pattern representative of a sequence of two or more frequencies at which said clock signal is required to be generated;

means for causing a clock generation element other than the clock generation element generating the clock signal at the immediately previous frequency in said sequence to generate a clock signal at a next frequency in said sequence;

means for causing the clock signal at the immediately previous frequency in said sequence to be disconnected from said clock output; and

means for causing the clock signal at the next frequency in said sequence to be connected to said clock output;

wherein the clock generation element being caused to generate a clock signal at each frequency in said sequence is independent of the value of said frequency.

2. (previously presented) The electronic device as recited in claim 1, wherein the clock signal at the immediately previous frequency in said sequence is caused to be disconnected from said clock output prior to connection of the clock signal at the next frequency in the sequence to said clock output.